DEC 0 6 2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Michael G. Monroe et al. Examiner: Jessica T. Stultz
Serial No.: 10/677,825 Group Art Unit: 2873
Filed: October 2, 2003 Docket No.: 200312474-1
Title: MEMS DEVICE AND METHOD OF FORMING MEMS DEVICE

DECLARATION OF PRIOR INVENTION UNDER 37 C.F.R. § 1.131

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir/Madam:

This Declaration is submitted to establish prior invention of the subject matter of the present patent application in the United States. The persons making this Declaration are the inventors, Michael G. Monroe, Eric L. Nikkel, Michele K. Szepesi, Stephen J. Potochnik, and Richard P. Tomasco.

Accompanying this Declaration are Exhibits A-D to establish reduction to practice of the subject matter of the present patent application prior to the earliest effective date of March 11, 2003 of U.S. Patent Application Publication No. 2003/0174934.

Exhibit A (2 pages) includes sketches and notes made by inventor Michael G. Monroe on October 2, 2002 illustrating the subject matter of the present patent application including processing steps incorporating sacrificial Silicon layers (i.e., polysilicon ("Si", "poly")) in accordance with the subject matter of the present patent application.

Exhibit B (1 page) includes an email of October 8, 2002 summarizing a "Process Brainstorm Meeting" attended by the inventors during which inventor Michael G. Monroe "proposed a process for producing a double decker structure using a 2 layer aluminum/sacrificial plasma silicon system" in accordance with the subject matter of the present patent application.

Exhibit C (20 pages) includes process details for Lot Number VME240509 as requested by inventor Michael G. Monroe and completed between October 4, 2002 and November 14, 2002. This lot includes processing steps incorporating a sacrificial Silicon layer (see, e.g., page 3) for producing parts in accordance with the subject matter of the present patent application.

Exhibit D (4 pages) includes an initial email of November 6, 2002 from inventor Michael G. Monroe giving an update on Phase 1 of the "Sacrificial Si" build (i.e.,

BEST AVAILABLE COPY

Lot#VME240509). Accompanying this email are images of parts from the build as formed in accordance with the subject matter of the present patent application.

From these exhibits, it can be seen that the subject matter of the present patent application was reduced to practice prior to the earliest effective date of March 11, 2003 of U.S. Patent Application Publication No. 2003/0174934.

As a person signing below, I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name: Michael G. Monroe Date: 11/29/04
Michael G. Monroe

Name: Date: 11/30/04
Eric L. Nikkel

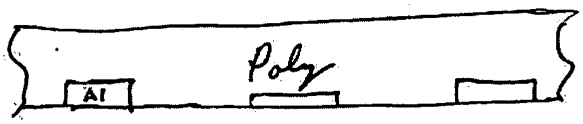
Name: Michele K Szepesi Date: 11|29|04
Michele K. Szepesi

Name: Date: 11/29/04
Stephen F. Potochnik

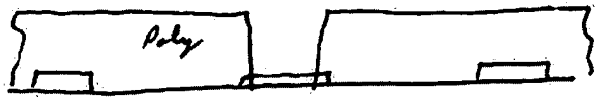
Name: Date: 29 Nov 2004
Richard P. Tomasco

OCT. 02, 2002 | SAC. POLY PROCESS | Michael D. Monroe

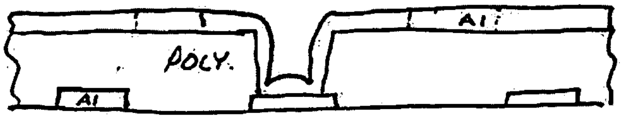
(A)



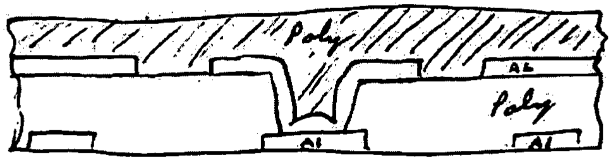
-400C PECVD Si Dep
- CMP of Si to Post height



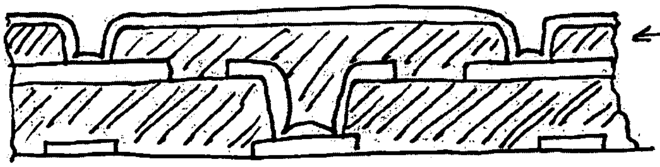
-Hinge photo & Si etch stop: on electrode (Al ?)



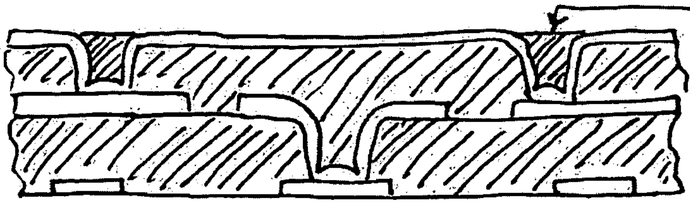
-Dep hinge level
- Pattern & etch hinge



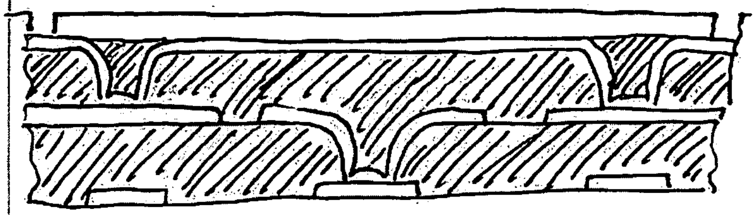
-Dep second level of Poly
-CMP Poly



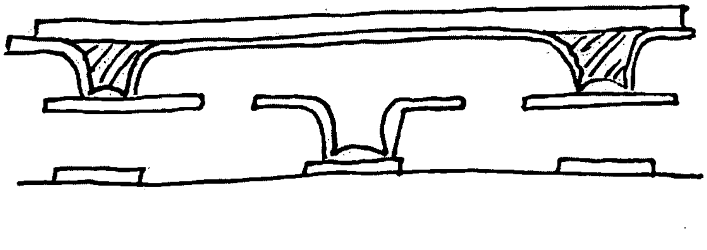
-MIRROR VIA PHOTO & ETCH
-Protection Al dep



-Dep Poly and CMP Back to Al to Fill Via



Dep and Pattern Al reflection layer



- Remove sac. Poly in Flourine Plasma

OCT. 02, 2002 | Michael G. Monroe

A

Big Question

- What material to use under electrode level to Protect CMOS ?
- Cl Plasma used in Al etch will also etch Si. How much can we stand, or do we care ?
- CMP of Poly and stopping on Al. How bad will Al look ? If we polish through Al can we stop on Poly ?
- What are things we can do to help contact resistance. Can we integrate Ti/TiN with sputter etch?
- Is this easier or harder than Metal on resist?
- How well can CMP hold post height thickness of Hinge level Poly? Also mirror Poly?
- What will the top Al look like after long Flourine Plasma exposure? Will it still be shiny.
- How long will the Flourine etch have to Be.
- How/what material for electrode coating

B

From: "NIKKEL,ERIC (HP-Corvallis,ex1)" [redacted]
To: "Potochnik, Stephen J" [redacted], "Monroe, Michael G." [redacted], "Tomasco, Richard P" [redacted], "Nikkel, Eric L" [redacted], "Szepesi, Mickey" [redacted]
Date: 10/8/02 4:37PM
Subject: Process Brainstorm Meeting Minutes

Here are the minutes of our FLE process brainstorm meeting held on October 2.

[redacted]

We began by walking through the TI process as we understand it and identified the following short loop activities:
1) Run short loop experiments aimed at learning how to coat sacrificial resist over an existing sacrificial resist layer. Steve will own this activity and will be designing and running short loop experiments for this learning.
2) Run short loop experiments aimed at learning how to pattern aluminum (over resist) using an oxide hardmask. Also to selectively remove the hardmask w/o damaging the exposed sacrificial resist. Eric will own this activity and will be designing and running short loop experiments for this learning.
3) Run short loop experiments aimed at learning how to ash hardbaked resist. This is assumed to be a challenge we will face due to the need to aggressively bake the 1st sacrifial layer in order to coat the next layer without interaction.
4) Run short loop experiments aimed at building double decker structures using the learnings from the above experiments. Steve and Eric will collaborate on this activity.

We then shifted the brainstorm to alternative processes for making double decker structures. Mike proposed a process for producing a double decker structure using a 2 layer aluminum/sacrificial plasma silicon system. It features a flat mirror surface produced with a plasma silicon "plug" filled mirror via. Mike will design and execute an experimetal build to investigate feasibility for this process.

Thanks to all for attending and contributing. -Eric.

CC: "Regan, Mike" [redacted]

FLE		QUESTIONS	**LOT NUMBER**	**VME240509**
		Gail Brooks		C
		X5-9036		

Short Loop	Entity	Time	Date	Initial	# Wfrs

Lot Number: OK — Red = Non-Default Processing Required

				Entity....................	Time..	Date.	Initials	#Wfrs
INV2LOT	1431	RAWINV2LOT	STOCKROOM FOR ALL INVENTORY	0396-IM				

Comments:

LIR#:

STA99SP	1470	STA99SCRIB	LASER SCRIBE	Marks2	1336		as	25
	1469	STA99SCCLN	LOT START SCRIBE CLEAN	OTS1	4:07	10/4	as	25
	1468	STA99CREAT	LOT START LOT CREATE	[illegible]S1	1445	10/4	[illegible]	25
	324	MVNSHOLD @ MVOU	STASP DONE LOTS					

MVNS
From Op. 324
To Op. 1764
Route: PL140DD

Done as

Comments:

LIR#:

PL140DD	1764	PL140DO SEETRVLR @MVIN	INTERMETAL DEPOSITION	88A	0639	10/8	[illegible]	25

Please deposit 5000A TEOS. No need for any metrology.
This is just a "base layer" for the short-loop
Any questions please contact Michael Monroe x56945, Cell 609-0141

After processing at operation 1764 a move non-standard is required.
MVNS
From Op. 1764
To Op. 1976
Route: MT2XXMD

Comments:

LIR#:

FLE		**QUESTIONS**	**LOT NUMBER**	**VME240509**
		Gail Brooks		
		X5-9036		

Short Loop	Entity	Time	Date	Initial	# Wfrs

MT2XXMD	1976		Metal 2 Metal Dep	END-62	0845	10-9	JB	25

DO NOT PROCESS AT OPERATION 1976.
PLEASE PUT LOT ON HOLD AND CONTACT ~~MICHAEL MONR~~OE @ 5-6945.

Deposit 4500A AlCu Confirmed with mm will set up new Recipe. JB 10-8
AlCu Dep Time 25.1 sec.

(RUN ON END-62 AND USE RECIPE ~~M1FLE~~ - ~~this recipe has been used for TiN~~) 10/8 @ 17
Run: END-62 AL 4500A 150C JB

After processing at operation 1976 a move non-standard is required.
MVNS
From Op. 1976 ✓ moved 1100 10/9 JB
To Op. 1931
Route: PL4VMDD

Comments:

LIR#:

(25)

FLE		**QUESTIONS**	**LOT NUMBER**	**VME240509**
		Gail Brooks		
		X5-9036		

Short Loop	Entity	Time	Date	Initial	# Wfrs

PL4VMDD	1931	FLEPL4DD SEETRVLR @MVIN	INTERMETAL DEPOSITION	AMT 82C	1540	10/13	Eddy	25

Do not process at operation 1931.
Please put lot on hold and contact Michael Monroe @ 5-6945.

Need 1.5 um 400C AMAT Si.

After processing at operation 1931 a move non-standard is required.
MVNS
From Op. 1931
To Op. 2216
Route: F21XXCMP

Comments:

SEQUENCE = X-SI X NH_3
recipes = X-SI X NH_3
NF_3 CLEAN COAT
} at 400°C

* 50Å/SEC dep rate

$\frac{15000Å}{50Å/SEC}$ = 300 SEC dep

300 x 1.2 = 360 sec clean

* No metrology recipe on 1280 would work used. dep rate given in TR 6202

Same SEQUENCE (recipes) used for Mickey's wf

complete write up found in TR #6202 — Eddy

LIR#:

FLE		QUESTIONS	**LOT NUMBER**	**VME240509**
		Gail Brooks		
		X5-9036		

Short Loop	Entity	Time	Date	Initial	# Wf

F21XXCMP	2216		GENERIC CMP	CMP-N03	16:00	10/17	MGM	20

Do not process at operation 2216.
Please put lot on hold and contact Michael Monroe @ 5-6945.

After processing at operation 2216 a move non-standard is required.
MVNS
From Op. 2216
To Op. 3072
Route: F21XXPH

Polished wafers for 30s. Should be about 1um of Poly left.

Comments:

Scrapping out wafers 1-5 for engineering experiments

LIR#:

FLE		**QUESTIONS**		**LOT NUMBER**		**VME240509**		
		Gail Brooks						
		X5-9036						
Short Loop			Entity		Time	Date	Initial	# Wfrs

F21XXPH	3072		NON-STANDARD PHOTO	N-P11	1035	21	wn	20

Do not process at operation 3072.
Put lot on hold and contact Rich Tomasco @ 5-3757 Done Bf LIR# 16147

Note that this is the First Expose.

Completed @ N-P11 R

Operation Description = Mirror Via Photo

Use the Nikon Body 11 and 60A. ✓
Use Linked Recipe 2 ✓
Use DMDB64AAHA ✓ reticle. Exposure= 195msec. ✓ — Per Rich T. See LIR
Use DMDB.MVA Nikon job file. ✓

After processing at operation 3072 a move non-standard is required.
MVNS
From Op. 3072 Insp = MVA -B64HA R
To Op. 1776
Route: VA140IE (Bay 4)

Comments:

LIR#:

FLE	**QUESTIONS**	**LOT NUMBER**	**VME240509**
		Gail Brooks	
		X5-9036	

Short Loop	Entity	Time	Date	Initial	# Wfrs
			Oct		

VA140IE	1776	VA140HB SEETRVLR @ MVIN	VA1 UV HARD BAKE	UV-71	1315	22	+	25

Do not process at operation 1776.
Please put lot on hold (in Bay 7) and contact Michael Monroe @ 5-6945. 609-0141

This is a short loop lot, and there is no topography yet. This is the first etch for mirror via. Should be etching through 10,000A Si and stopping on 4500A of Al

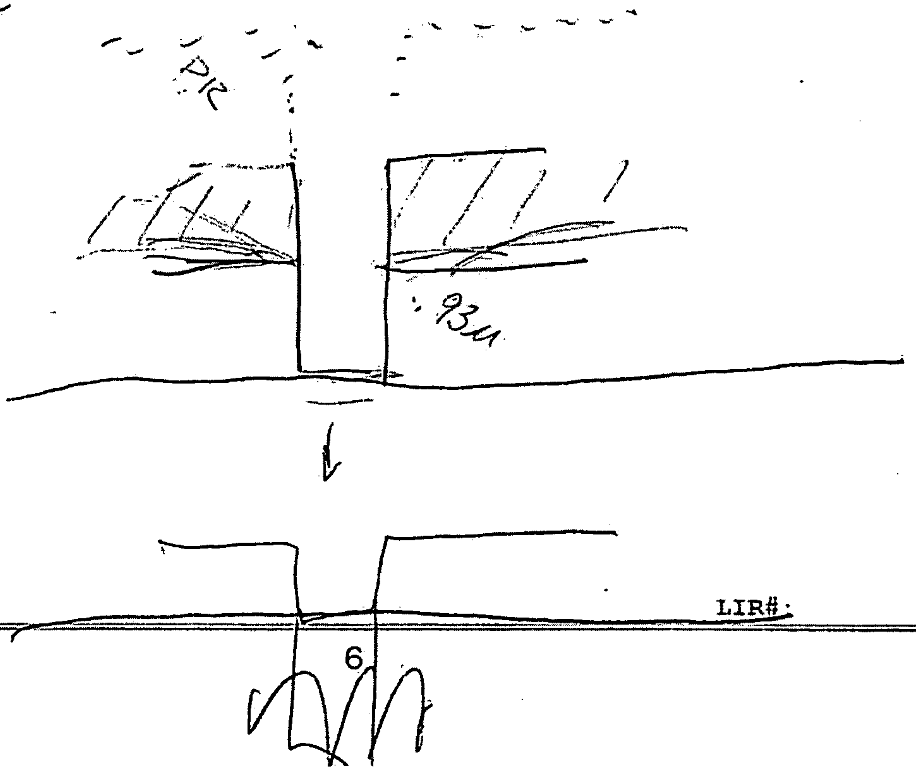
Rec. 109	1777	VA140PE	VA1 PLASMA ETCH	4520-81	4:45	10/22	GW	19
	1778	VA140MEPT	VA1 ETCH ENDPOINT	150				
	1779	VA140AS	VA1 ASH	Ash. 45	1945	10/22	JP	19
	1780	VA140ST	VA1 STRIP	STRIP. 71	2055	10/22	JP	19
	1781	VA140RD MVNSHOLD@ MVOU	VIA 1 RINSE/DRY	RD. 76	2115	10/22	JP	19

After processing at operation 1781 a move non-standard is required.
From Op. 1781
To Op. 1976
Route: MT2XXMD MOVED

Comments:

→ Need to [illegible] sell wafer #24 to Eng.

PUT IN LAMSTN-74
@ ENDPOINT 60SEC



LIR#:

FLE		**QUESTIONS**	**LOT NUMBER**		**VME240509**	
		Gail Brooks				
		X5-9036				
Short Loop			Entity	Time	Date	Initial	# Wfrs

MT2XXMD	1976	M1AL	Metal 2 Metal Dep	MRC-63	1057	10/23	[illegible]	19

Do not process at operation 1976.
Put lot on hold and contact Michael Monroe @5-6945 voicemailed 2255 GB:

Deposit 5000A AlCu. → MRC-63 RECIPE = M1AL

After processing at operation 1976 a move non-standard is required.
MVNS
From Op. 1976
To Op. 3072
Route: F21XXPH

Comments:

LIR#:

FLE		QUESTIONS	**LOT NUMBER**	**VME240509**
		Gail Brooks		
		X5-9036		

Short Loop	Entity	Time	Date	Initial	# Wfrs
					19

F21XXPH	3072		NON-STANDARD PHOTO	13	17:01	10/24		

Do not process at operation 3072.
Put lot on hold and contact Rich Tomasco @ 5-3757

Operation Description = Mirror Photo

DI #08, 25

Use DMDB61ABFA reticle. Exposure= ~~175~~ 190msec.
Use DMDB.MIR job file.
Use default coat and develop recipe. -31

Many PSG particles noted.

After processing at operation 3072 a move non-standard is required.
MVNS
From Op. 3072
To Op. 3061
Route: F21XXME (BAY 6)

Comments:

LIR# 16559

LIR#:

FLE	QUESTIONS	**LOT NUMBER**	**VME240509**
	Gail Brooks		
	X5-9036		

Short Loop				Entity	Time	Date	Initial	# Wfrs
F21XXME	3061		GENERIC METAL ETCH	9bSE-71-2	12^{00}	11/4	JL	19

Do not process at operation 3061.
Put lot on hold and contact Michael Monroe @ 5-6945.

Mike will work with John Williams for the etch.

Comments:

Done

LIR#:

~~**Please deliver lot to Support.**~~
~~Support: please sell wafers to costcenter 6410533900, put them in a white boat and tape the box. Also call Gail Brooks @ 5-9036 for pick up. Thanks!!~~

FLE	QUESTIONS	**LOT NUMBER**	**VME240509**
	Gail Brooks		
	X5-9036		

Short Loop	Entity	Time	Date	Initial	# Wfrs

PL4VMDD	1931	FLEPL4DD SEETRVLR @MVIN	INTERMETAL DEPOSITION	82C	313	11-5	w	~~19~~

14

Do not process at operation 1931.
Please put lot on hold and contact Michael Monroe @ 5-6945.

Need 1.5 um 400C AMAT Si. X-NH3 CT 400 DEG

After processing at operation 1931 a move non-standard is required.
MVNS
From Op. 1931 Redep per Mike Monroe
To Op. 2216
Route: F21XXCMP

Comments:

LIR#:

FLE		**QUESTIONS**	**LOT NUMBER**	**VME240509**
		Gail Brooks		
		X5-9036		

Short Loop	Entity	Time	Date	Initial	#Wf

F21XXCMP	2216		GENERIC CMP	CMP-N03	17:00	11/7	MGM	11

Do not process at operation 2216.
Please put lot on hold and contact Michael Monroe @ 5-6945.

After processing at operation 2216 a move non-standard is required.
MVNS
From Op. 2216
To Op. 3072
Route: F21XXPH

AFTER SECOND DEPOSITION, POLISHED WAFERS FOR 100S. SCRAPPED TWO WAFERS FOR ENGINEERING TESTS

Comments:

Ready for VIA PHOTO with Mickey

Mike Monroe 11/7/02

* lot sold off W/S 11/18 due to alignment issues @ Mirror Via photo. Found out tool had issues and now lot being recreated as child lot - see next page

LIR#:

FLE		QUESTIONS	**LOT NUMBER**	**VME240509A**
		Gail Brooks		
		X5-9036		

Short Loop	Entity	Time	Date	Initial	# Wfrs
					11

F21XXPH	3072		NON-STANDARD PHOTO					

Do not process at operation 3072.
Put lot on hold and contact Rich Tomasco @ 5-3757

Operation Description = Mirror Via Photo (ALIGNS → MVA TARGETS)
Rich - this lot will need a manual offset alignment

Use the Nikon Body 11 and 60A.
Use Linked Recipe 2 12/32
Use DMDB64AAHA reticle. Exposure= 195msec.
Use DMDB.~~MVA~~ ~~MIR~~ Nikon job file. ~~MVA_TARGS JOBFILE~~ USE DMDB.MIR

After processing at operation 3072 a move non-standard is required.
MVNS
From Op. 3072
To Op. 1776
Route: VA140IE

Comments:

RAN NEW PHOTO JOB TO CLEAR OUT ALIGNMENT TARGETS FOR MVA LEVEL TARGS.
COATED 1.8u 3615 DNS 60A P-11 (12/32)
EXPOSED OPEN FRAME w/ DMDB.MVA_TARGS JOBFILE @ 200 MS
- MIKE MONROE TO SF6 ETCH BLANKET EXPOSED FIELDS AND RETURN LOT FOR MIRROR VIA PHOTO PROCESSING.

R TOMASCO
14 NOV 2002

LIR#:

FLE		**QUESTIONS**	**LOT NUMBER**	**VME240509A**
		Gail Brooks		
		X5-9036		

Short Loop	Entity	Time	Date	Initial	#W

VA140IE	1776	VA140HB SEETRVLR @ MVIN	VA1 UV HARD BAKE					

Do not process at operation 1776.
Please put lot on hold (in Bay 4) and contact Curt Voss @ 5-1782.

	1777	VA140PE	VA1 PLASMA ETCH					
	1778	VA140MEPT	VA1 ETCH ENDPOINT					
	1779	VA140AS	VA1 ASH					
	1780	VA140ST	VA1 STRIP					
	1781	VA140RD MVNSHOLD@ MVOU	VIA 1 RINSE/DRY					

After processing at operation 1781 a move non-standard is required.
From Op. 1781
To Op. 3062
Route: MT3XXMD

Comments:

LIR#:

FLE	QUESTIONS	LOT NUMBER	VME240509A
		Gail Brooks	
		X5-9036	

Short Loop	Entity	Time	Date	Initial	# Wfrs

MT3XXMD	3062		Generic Metal Dep					

Do not process at operation 3062.
Put lot on hold and contact Michael Monroe @5-6945

Need 3500A AlCu

After processing at operation 3062 a move non-standard is required.
MVNS
From Op. 3062
To Op. 1931
Route: PL4VMDD

Comments:

LIR#:

FLE		QUESTIONS		**LOT NUMBER**		**VME240509A**	
		Gail Brooks					
		X5-9036					
Short Loop			Entity	Time	Date	Initial	#W.s

PL4VMDD	1931	FLEPL4DD SEETRVLR @MVIN	INTERMETAL DEPOSITION					

Do not process at operation 1931.
Please put lot on hold and contact Michael Monroe @ 5-6945.

Need 2.0 um 400C AMAT Si.

After processing at operation 1931 a move non-standard is required.
MVNS
From Op. 1931
To Op. 2216
Route: F21XXCMP

Comments:

LIR#:

FLE		QUESTIONS	**LOT NUMBER**	VME240509A
		Gail Brooks		
		X5-9036		

Short Loop	Entity	Time	Date	Initial	# Wfrs

F21XXCMP	2216		GENERIC CMP					

Do not process at operation 2216.
Please put lot on hold and contact Michael Monroe @ 5-6945.

After processing at operation 2216 a move non-standard is required.
MVNS
From Op. 2216
To Op. 3062
Route: MT3XXMD

Comments:

LIR#:

FLE		QUESTIONS	**LOT NUMBER**	**VME240509A**
		Gail Brooks		
		X5-9036		

Short Loop	Entity	Time	Date	Initial	#Wi

MT3XXMD	3062		Generic Metal Dep					

Do not process at operation 3062.
Put lot on hold and contact Michael Monroe @5-6945

Need 3500A AlCu

After processing at operation 3062 a move non-standard is required.
MVNS
From Op. 3062
To Op. 1931
Route: PL4VMDD

Comments:

LIR#:

FLE		QUESTIONS		**LOT NUMBER**				**VME240509A**
		Gail Brooks						
		X5-9036						
Short Loop				Entity	Time	Date	Initial	# Wfrs

F21XXPH	3072		NON-STANDARD PHOTO					

Do not process at operation 3072.
Put lot on hold and contact Rich Tomasco @ 5-3757

Operation Description = Mirror Photo

Use DMDB61ABFA reticle. Exposure= 175msec.
Use DMDB.MIR job file.
Use default coat and develop recipe.

After processing at operation 3072 a move non-standard is required.
MVNS
From Op. 3072
To Op. 3061
Route: F21XXME (BAY 7)

Comments:

LIR#:

FLE		QUESTIONS			**LOT NUMBER**	**VME240509A**
		Gail Brooks				
		X5-9036				frs
Short Loop			Entity	Time	Date	Initial	# Wfrs

F21XXME	3061		GENERIC METAL ETCH					

Do not process at operation 3061.
Put lot on hold and contact Michael Monroe @ 5-6945.

Mike will work with John Williams for the etch.

Comments:

LIR#:

Please deliver lot to Support.
Support: please sell wafers to costcenter 6410533900, put them in a white boat and tape the box. Also call Gail Brooks @ 5-9036 for pick up. Thanks!!

DMDBA00C00

FLE

QTY: 11

QUESTIONS
GAIL BROOKS
X59036

LOT# VME240509A

Lot Number:	VME240509A	**FLE**
Qty:	11	
Wafers:		

Date	Init.			
		Product:	**DMDBA00C00** ✓	**Req. Engr: Mike Monroe**
		Owner:	**ENGR**	**Ext: 5-6945**
		Create Category:	**FLE**	**Process Engr contacts:**
		Priority:	**0**	**Ext:**
		Cost Center:	**6410533900** ✓	**Process Tech contacts:**
		Metric Attribute	**ND**	
		Resp. Person:	**GB/Monroe**	**Operation Specialist: Gail Brooks**
		Request Number:	**27390**	**Ext: 5-9036**
		Start Material:	**VME240509-** **Lot in Support** ✓	**Pgr: 757-6074**
		Starting Route:	**F21XXPH** ✓	
		Starting Operation:	**3072**	**Objective: FLE Micromirror Shortloop**
		FCM Request #	N/A	Start Date:
		IB2 (MAPBASE)	N/A	Require Date:
				[ ] Full Process [X] S - Loop B

Date	Init.	**Special Instructions:**
		SUPPORT- Parent lot was sold off workstream - need to recreate it and send lot for more processing

For **URGENT** needs, please leave **URGENT** voicemail by pressing #/1/2 after your message and I will be paged automatically. **OR Alpha page** me via the WEB URL **http://protowww.cv.hp.com/proto/**
Thank you, Gail Brooks x59036 pgr. 757-6074

D

From: "REGAN,MIKE (HP-Corvallis,ex1)" [redacted]
To: [redacted]
Date: 11/8/02 11:09AM
Subject: RE: Phase 1 of Sacrificial Si build looking great! (Lot#VME240509)

Great job team. This is a big achievement on the process side. The success of this effort, in terms of the Si deps, CMP, photo/etch, SF6 wafer release, integration, etc., gives me great confidence in our organization to move quickly and intelligently to sort out difficult problems.

We will be anxiously waiting the next results. Good luck.

Mike

-----Original Message-----
From: MONROE,MICHAEL G (HP-Corvallis,ex1)
Sent: Wednesday, November 06, 2002 6:32 PM
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Subject: Phase 1 of Sacrificial Si build looking great! (Lot#VME240509)

Hi All,

Just wanted to send out a quick update on the sacrificial silicon build I've been working on in the fab. Take a look at the pictures in the attached word file.This shortloop has blanket AlCu covered with the PECVD Si deposition. (Actually being able to deposit this Si material on AlCu was a first. (Thanks to Jenny Shih and Eddy Hanson for the new Si dep material.) Once the wafers were done with dep., I was able to polish the Si without seeing any delamination. (Another first for Si on AlCu.!.) We then patterned and etched the wafer with Mirror via. (Thanks to Curt Voss for the Si Via etch). We then depped 5000A of AlCu for the mirror/hinge and patterned. (Thanks to Rich Tomasco. for Photo, and John Williams for the metal etch). We then etched the wafers in an SF6 plasma for the mirror release etch. Attached are picture of the mirrors after release. (Thanks to Dennis Lazaroff for the SF6 etch help and the fine SEM work) As you can see from the pictures, the mirrors are very flat and fully released. This was the first time we have released flat AlCu mirrors at the wafer level, ever! The bigger deal, is that we were able to do this in a 5min. etch for the whole wafer. More characterization is underway by Dennis to determine Si etch rates vs. TEOS.

This is basically phase 1 of the shortloop. I am trying to build a double decker structure with the rest of the wafers, with the addition of a Si plug process that will allow us to fill the mirror via to produce a perfectly

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flat top mirror. I will send out a VISO file of the process flow soon, and more updates as I learn more.

Also, many thanks to Chris Leonard for his expert etch advice, Gail Brooks for the lot traveler assembly, Mickey Szepesi, Eric Nikkel, Steve Potochnik for their process integration help, and the PDO operations staff in the fab who helped me along with my lot.

regards,

Michael G. Monroe
Hewlett Packard
Process Integration Engineer
Corvallis, OR.

[redacted]

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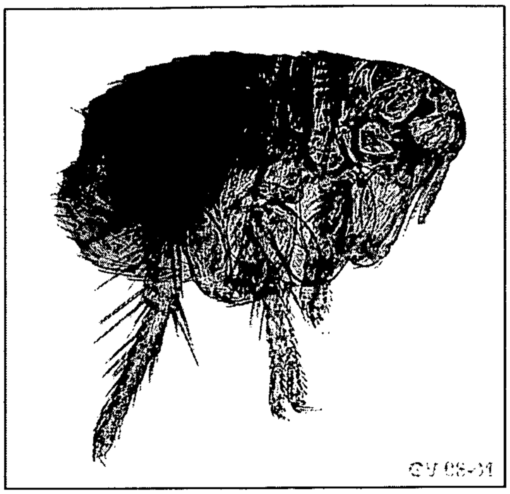
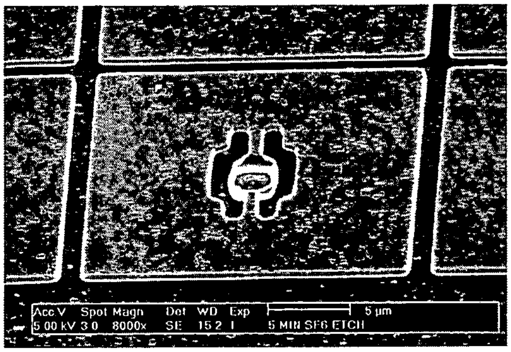


This is a Flea…


Acc.V Spot Magn Det WD Exp 5 µm
5.00 kV 3.0 8000x SE 15.2 1 5 MIN SF6 ETCH

This is a FLE mirror… Any questions??? :^)

Ok… keep scrolling down to the next page to see the pictures…

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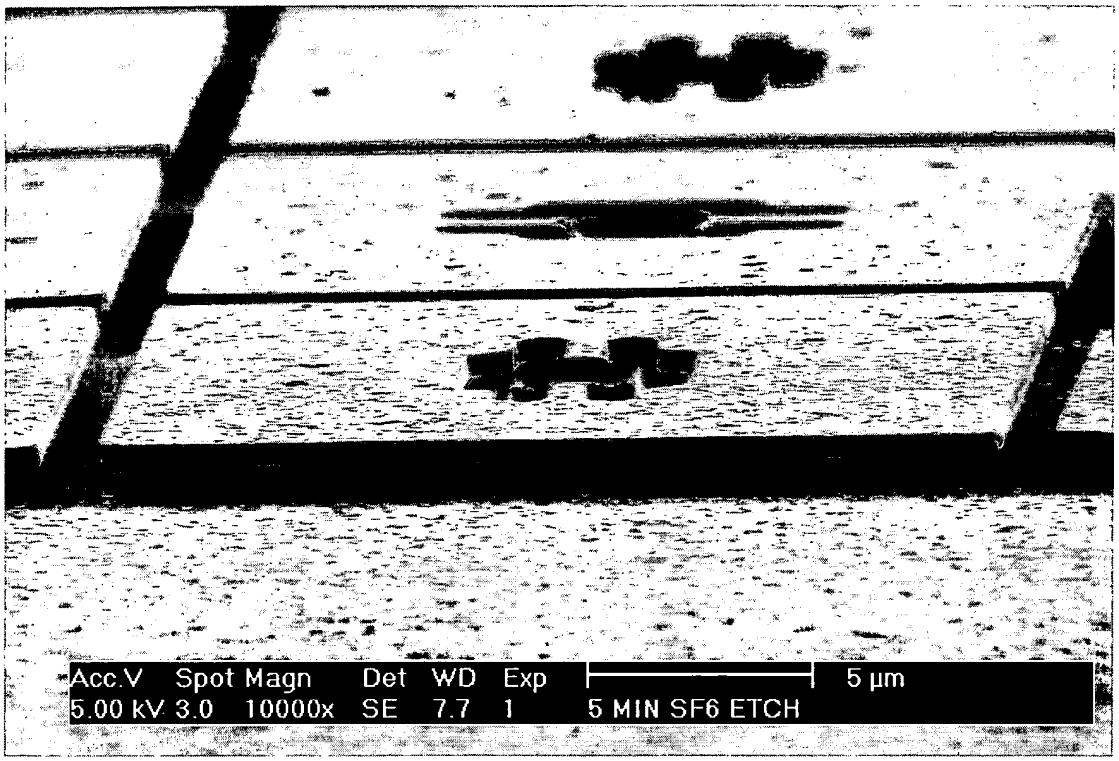
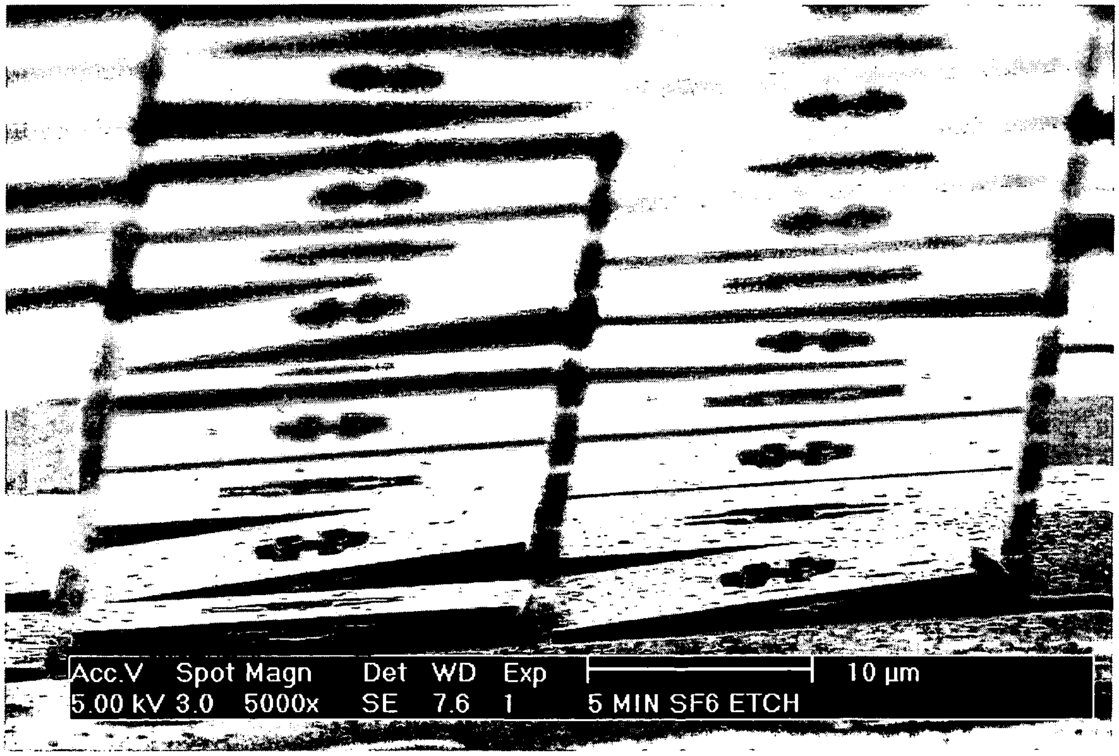

Acc.V Spot Magn Det WD Exp 5 µm
5.00 kV 3.0 10000x SE 7.7 1 5 MIN SF6 ETCH

Here is a great 80deg. tilt view of a released mirror. All the mirrors look pretty flat, and are fully released.
(5min. etch at wafer level is pretty sweet, from a manufacturing standpoint!)


Acc.V Spot Magn Det WD Exp 10 µm
5.00 kV 3.0 5000x SE 7.6 1 5 MIN SF6 ETCH

One more picture after putting some alcohol on the wafer to get the mirrors to tilt and stick down. You can see under the bottom left mirror that the Si is all gone…

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